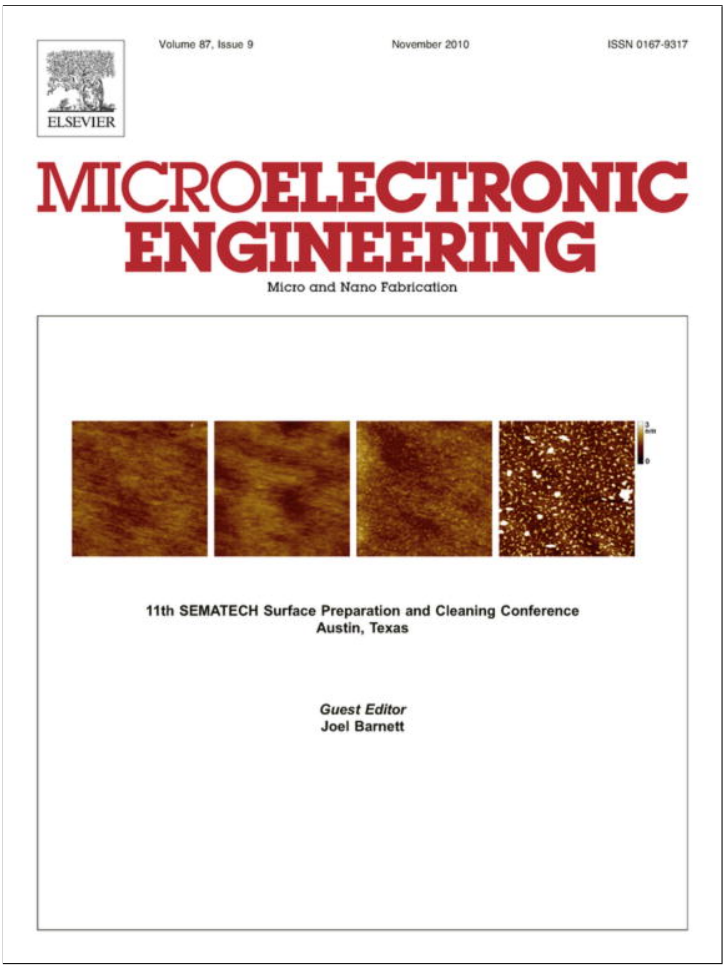

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Intra-level voltage ramping-up to dielectric breakdown failure on Cu/porous low-*k* interconnections in 45 nm ULSI generation

C.H. Huang [a], N.F. Wang [b], Y.Z. Tsai [b], C.I. Hung [c], M.P. Houng [a,*]

[a] *Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Taiwan*
[b] *Department of Electronic Engineering, Cheng Shiu University, Taiwan*
[c] *Department of Mechanical Engineering, National Cheng Kung University, Taiwan*

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ABSTRACT

The degradation of reliability for intra-level voltage-breakdown in the 45 nm generation node has become an increasingly important issue with the introduction of porous low-*k* dielectrics. The dominant failure mechanism for lower voltage ramping-up to dielectric breakdown and higher leakage current was that more electrons easily transported through the percolation path in intra-level porous low-*k* interconnections damaged from HF corrosion. An optimal ultraviolet curing process and a less NH_3 plasma pretreatment on porous low-*k* dielectrics before the SiCN capping layer are developed to improve performance in both of these cases. The stiff configuration of the reconstruction of Si–O network structures and less HF corrosion is expected to have high tolerance to electrical failure. As a result, the proposed model of this failure facilitates the understanding of the reliability issue for Cu/porous low-*k* interconnections in back-end of line (BEOL) beyond 45 nm nodes.

1. Introduction

As the size of integrated circuit features shrinks, the interconnect widths become smaller; therefore, signal propagation delays become a dominant part of the overall chip delay. Cross-talk and power consumption greatly increase due to the parasitic capacitance of interlayer dielectrics and the resistance of wiring metals. Moreover, inter-level or intra-level dielectric reliability issues have become an increasingly crucial concern in addition to increasing process complexity. Major reliability issues of back-end of line (BEOL), such as electro-migration (EM), stress migration (SM), voltage ramping-up to dielectric breakdown, and time-dependent dielectric breakdown (TDDB), have received more attentions in Cu damascene architectures. Cu ions can easily diffuse into interconnecting insulators in the absence of a metal barrier or an oxide barrier when an electric field is applied.

The failures of inter-level dielectric reliability in Cu damascene architecture have been reported. Some researches reported that the intrinsic properties of the dielectrics contribute to the degradation of reliability [1,2]. "Intrinsic", denotes that the material properties and integration strategy are used in the formation of BEOL, including Cu and low-*k* dielectrics. Gonella et al. [1] reported that the presence of Cu contamination gives rise to a significant leakage current. Ogawa et al. [2] reported that a porous silica-base low-*k* film resulted in the degradation of E_{bd} and TDDB. Other researchers have emphasized the reliability issues related to the interface between the inter-level dielectrics and the oxide diffusion barrier [3,4]. Alers et al. [3] reported that the reliability failure of the interconnection strongly depends on the properties of the dielectric diffusion barrier because the adhesion energy between Cu and the dielectric barrier, and the mechanical strength of the dielectric barrier are two crucial parameters. Noguchi [4] reported that Cu ions migrate along the dielectric surface due to heavier metal residues from the Cu CMP, resulting in the degradation of dielectric reliability.

A popular strategy for reducing the dielectric constant of a silica-based matrix is to add porosity into it. The added pores can be formed through self-organization of the material, such as a termination (Si–CH_3 or Si–H) or, can be formed through the selective removal of part of the material. The latter is a novel and advanced technology in recent IC fabrication. The purpose for the introduction of porogen organic chemicals into low-*k* dielectrics is to create a greater porosity by using ultraviolet (UV) irradiation curing or other technologies, such as thermal annealing or E-beam, to remove them to reach a lower dielectric constant [5–9]. However, this new approach rise more challenges for the reliability of intra-layer voltage-breakdown in or beyond 45 nm generation devices. In this paper, we explore the failure model of voltage ramping-up to dielectric breakdown from fabricated integrations in the Cu/porous low-*k* interconnections of 45 nm generation devices.

* Corresponding author. Tel.: +886 6 275 7575x62342; fax: +886 6 234 5482.
E-mail address: mphoung@eembox.ncku.edu.tw (M.P. Houng).

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2. Experiment

Fig. 1 shows single Cu damascene process flows in a standard interconnection of BEOL fabrication. First, three dielectric films, SiCN film (silicon carbide doped nitride film), porous low-*k* SiOCH films ($k = 2.5–2.6$), and a hard mask layer, were deposited subsequently using plasma-enhanced chemical vapor deposition (PECVD) and physical vapor deposition (PVD), followed by trench lithography and etching processes. Porogen-based porous low-*k* SiOCH films were used in UV curing with a wavelength at the range of 200–300 nm to remove the organic porogen. The UV curing time was examined because the film properties correspond to UV curing behavior. In these experiments, the UV curing time varied around a reference time, "*T*", which was 7 min, from 1 to 3*T*. The etching steps used fluorine-based chemistries to define the trench profile and the following ash steps used CO/O_2 and He/H_2 chemistries to remove photo resist, respectively. Conventional metallization including TaN/Ta barrier, Cu seed and Cu electrochemical deposition was then carrier out on the patterned dielectric. Then, the wafers were followed by Cu chemical–mechanical polishing (CMP). After CMP process, thermal annealing was performed to control Cu stress and to clean the impurity residue. NH_3 plasma pre-treatment was employed on the surface of the underlying layers before dielectric diffusion barrier deposition, followed by SiCN dielectric film deposition. A previous study [10] reported that NH_3 plasma treatment can be applied to improve the quality of the interface between a barrier dielectric and the underlying films, including Cu wire and porous low-*k* dielectrics.

The film thickness and refractive index (at a 632.8 nm wavelength) were measured on an optical-probe system with an ellipsometer. The shrinkage ratio of the thickness was determined by the difference of the film thickness for different UV curing times. Chemical bonding of the SiOCH films was characterized using Fourier transform infrared (FTIR). FTIR spectroscopy measurements, using a Bio-Rad's QS2200 system, within a range from 400 to 4000 cm^{-1}. Hardness and Young's modulus were determined using nano-indentation. Dielectric constant was obtained at a frequency of 1 MHz using capacitance–voltage (*C*–*V*) methods (HP-4284 C-V system) at the accumulation region with a metal–oxide-semiconductor (MIS) structure. After finishing the IC fabricated processes, series electrical characterizations were performed on the patterned wafer-level to evaluate its impact. Electrical characterizations such as copper line resistance, line-to-line leakage current, and voltage ramping-up to dielectric breakdown were measured using serpentine/comb test structure. For the voltage ramping-up to dielectric breakdown test, the applied voltage to the dielectrics was uniformly stair-step upwards in a fixed voltage. Transmission electron microscopy (TEM) was used for failure analysis (FA).

3. Results and discussion

The bonding structures and film properties of the porous low-*k* SiOCH materials with the various UV curing conditions are examined in this study. The UV curing times were varied around a reference time, *T* (of the magnitude of 7 min). Following different curing splits, a variety of material's characterization techniques were used to investigate film properties. Several studies [11–13] reported that the variation of these bonding structure changes of porous low-*k* materials with various UV curing times are related to the chemical reactions on these films during UV irradiation curing. The FTIR spectra of porous low-*k* films distributed upon different UV curing time are shown in Fig. 2a. It features the following absorptions: network Si–O–Si stretching (~1060 cm^{-1}); cage-like Si–O–Si stretching (~1150 cm^{-1}); Si–O–Si bending (~440 cm^{-1}); CH_3 symmetric bending in $Si–(CH_3)_x$ (~1270 cm^{-1}); $C–H_x$ stretching (~2850–3100 cm^{-1}). The changes of these bonding structures of the porous low-*k* materials with different UV curing times were observed from FTIR spectra, we can infer the chemical reactions on these films during UV irradiation curing. The structure modification of Si–O–Si network structures comes from the reactions between cage-like structures and $Si–CH_3$ bonds [11–13]. The CH_x band over the range of 2750–3100 cm^{-1} comprises four hydrocarbon peaks, including the CH_3 asymmetric (~2970 cm^{-1}), CH_2 asymmetric (~2925 cm^{-1}), CH_3 symmetric (~2890 cm^{-1}) and CH_2 symmetric (~2875 cm^{-1}) vibrations, as shown in Fig. 2b. The peak area of $C–H_x$ stretching mode strongly decreased with the increase of UV curing time, as shown in Fig. 2c, indicating that organic species were removed from the film. We also believe that the

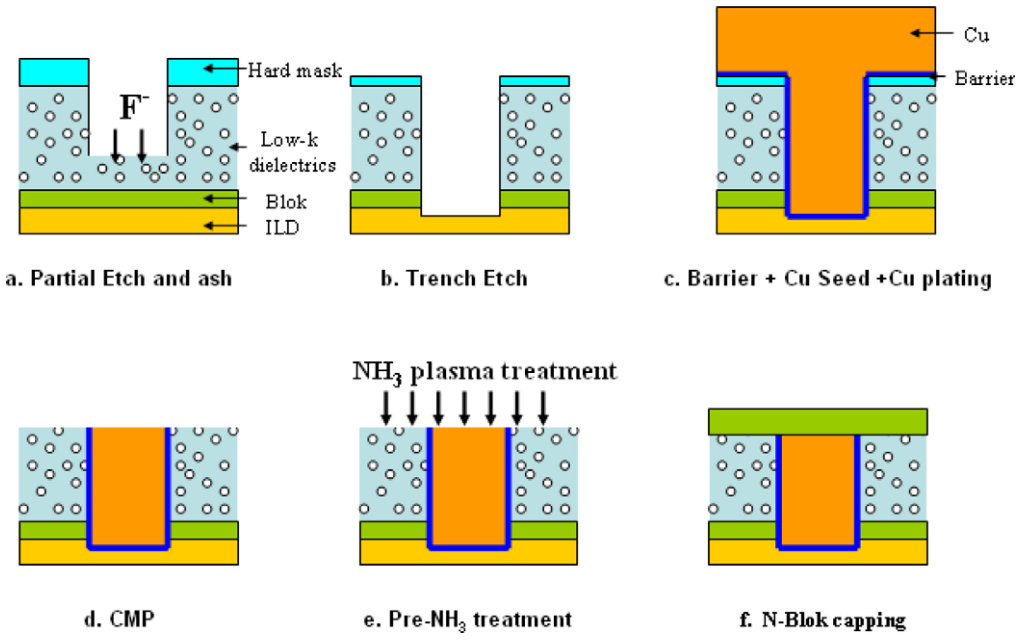

Fig. 1. Process flow of Cu single damascene wiring architecture.

variance of CH_x peaks provides evidence of the removal of the thermally unstable CH_x fragments from the mixture precursor [6,13]. Verdonck et al. [6] indicated that the removal of CH_2 groups increases the porosity and decreases the dielectric constant, and that the removal of the CH_3 groups increases cross-linking and hence probably decreases the porosity and increases mechanical

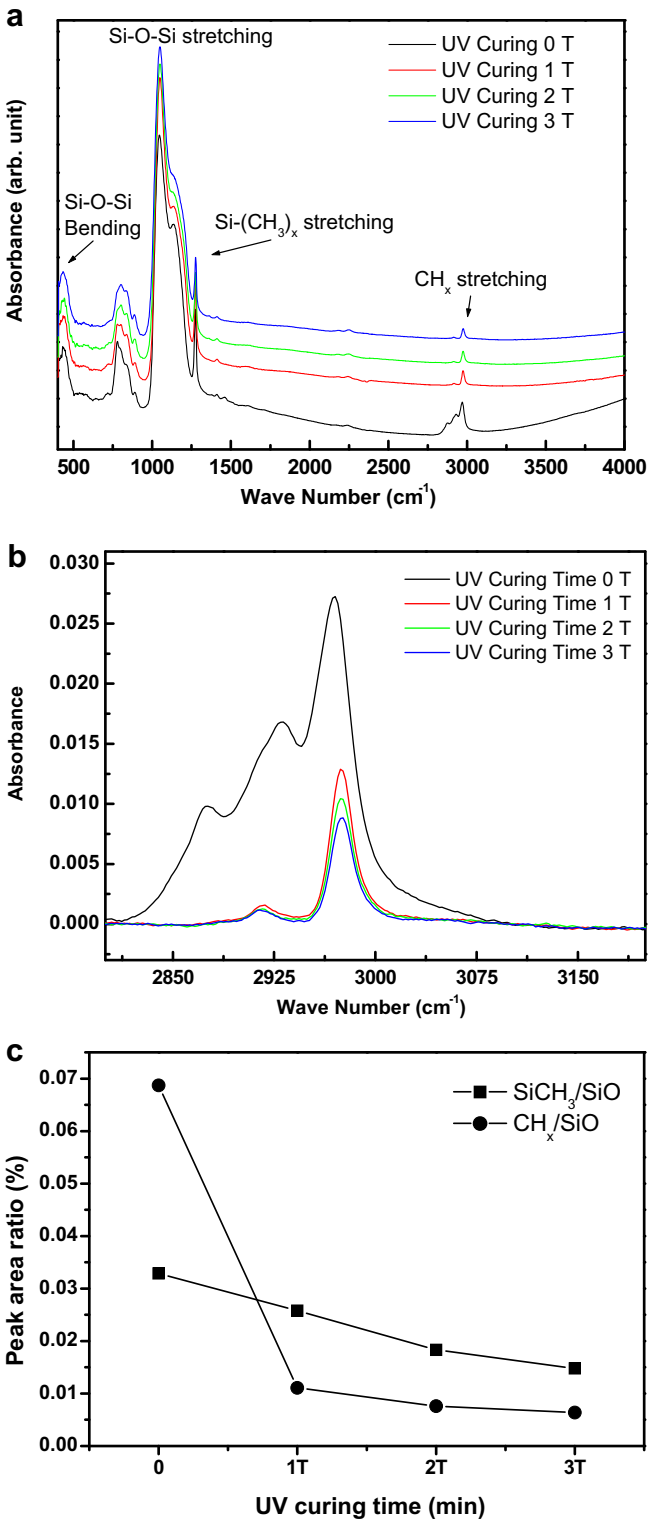

Fig. 2. (a) FTIR spectra within the range of 400–4000 cm^{-1} for porous low-*k* films distributed upon different UV curing time. ("*T*" expresses the UV curing time of 7 min), (b) the FTIR-spectrum peak distribution of the CH_x band at the range of 2750–3200 cm^{-1} for porous low-*k* films distributed upon different UV curing time. ("*T*" expresses the UV curing time of 7 min) and (c) the peak area ratios of $SiCH_3/SiO$ and CH_x/SiO for the low-*k* films.

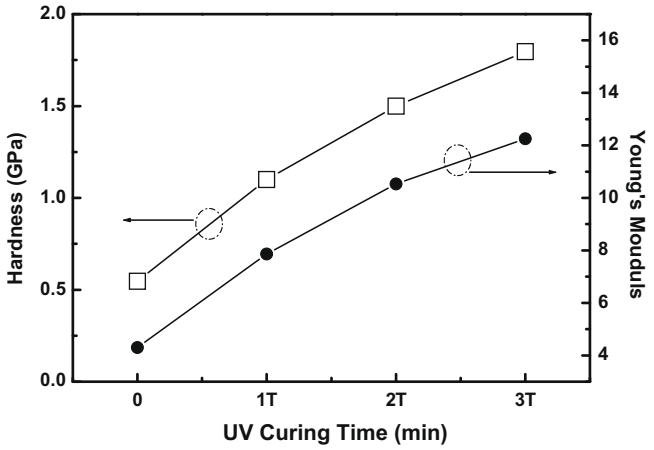

Fig. 3. Hardness and Young's modulus as a function of UV curing time.

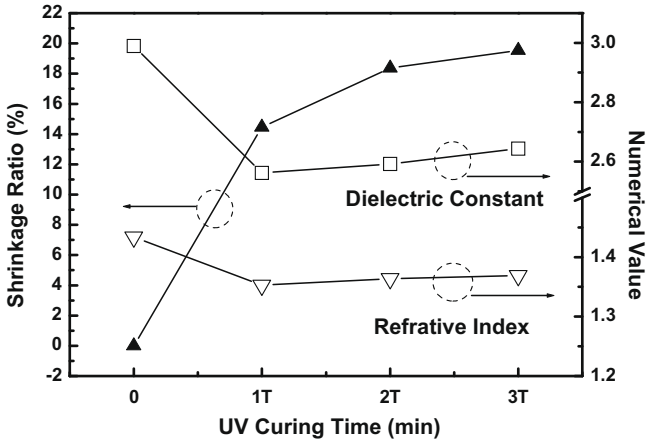

Fig. 4. The variation of shrinkage ratio, refractive index and dielectric constant with varying UV curing time for the low-*k* films.

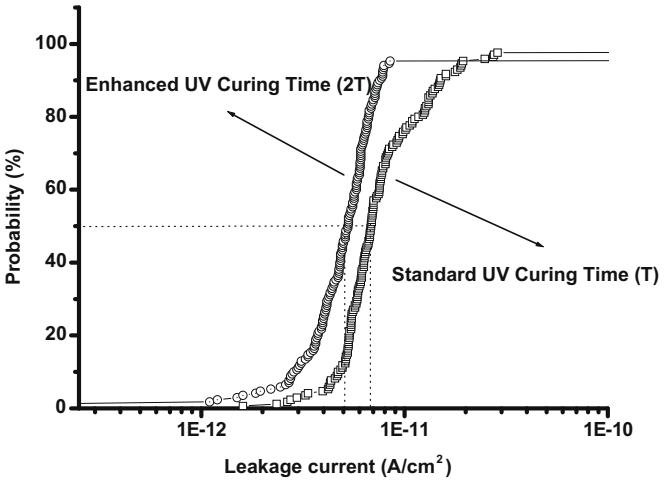

Fig. 5. The line-to-line current leakage distribution for standard UV cured (1*T*) porous dielectrics and enhanced UV cured (2*T*) porous ones at an applied electric field of 2 MV/cm.

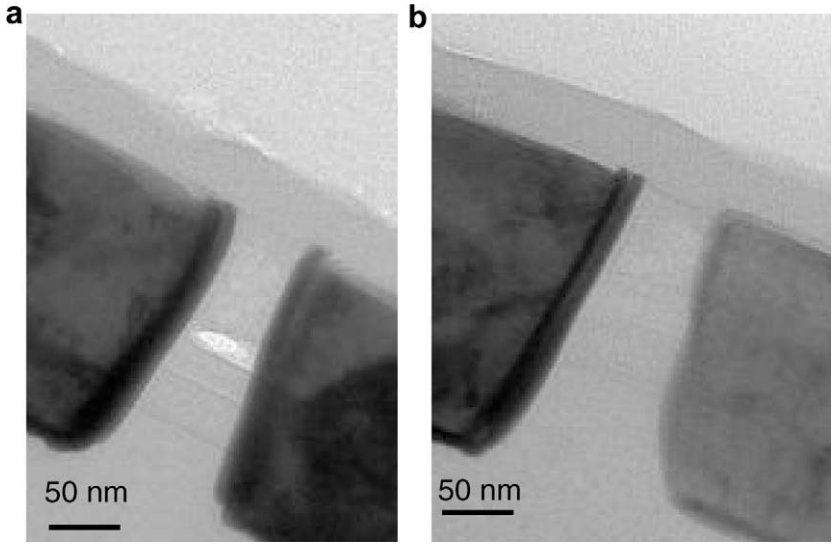

Fig. 6. The schematic diagrams of TEM cross-section for: (a) standard UV curing sample; (b) enhanced UV curing sample.

strength. Fig. 3 shows that mechanical strength, including hardness and Young's modulus, is as a function of the UV curing time. As a result, the removal of the unstable hydrocarbon (CH_x) groups further strengthens the structure configuration of the film and increases the film density.

Fig. 4 shows the variations of shrinkage ratio and refractive index of the porous SiOCH films using UV irradiation with various curing conditions from 1 to 3*T*. Several reports indicated that structure modifications of Si–O–Si suboxide bonds and Si–O–Si cage-like bonds turn into Si–O–Si network structures, subsequently dominating the variation of shrinkage ratio and refractive index on low-*k* materials because the average bond strength is intensified with increasing Si–O–Si bonds in the skeleton of the network that is produced by UV irradiation curing [14]. The changes of the dielectric constant of porous SiOCH materials for as-deposited film and UV irradiation with various UV curing time are also shown in Fig. 4. It can be concluded that the cross-linking structures and the removal of the organic CH_x phase through UV irradiation improve the mechanical and electrical properties of porous low-*k* SiOCH materials [15]. These results further demonstrate the relationship between electrical failure and intrinsic properties of the porous dielectrics.

Fig. 5 shows the distributions of the line-to-line leakage current of Cu wires (pitch/line = 124/66 nm) at an applied electric field of 2 MV/cm in room temperature. The enhanced UV curing sample

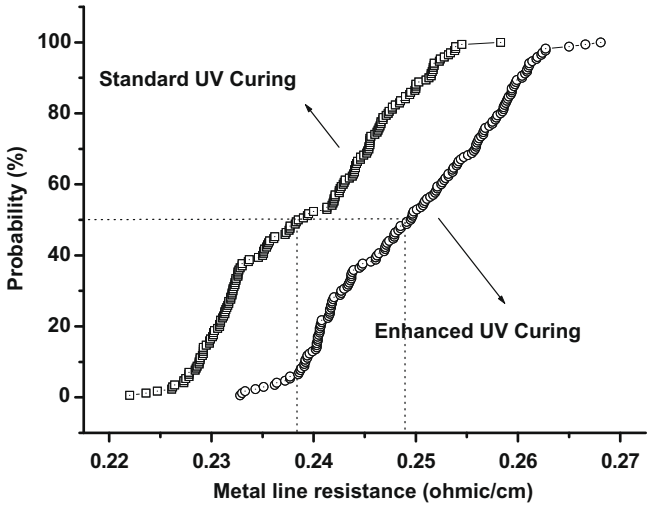

Fig. 7. The resistance of metal line distributions for standard UV cured (1 T) porous dielectrics and enhanced UV cured (2 T) porous ones. (The dimensions of the pitch and space are 124 and 66 nm, respectively).

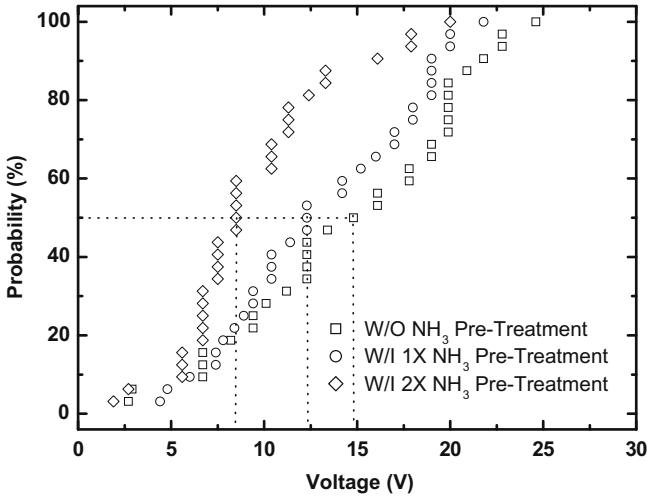

Fig. 8. The distribution of voltage ramping-up to dielectric breakdown for various NH_3 plasma pre-treatment conditions before SiCN capping.

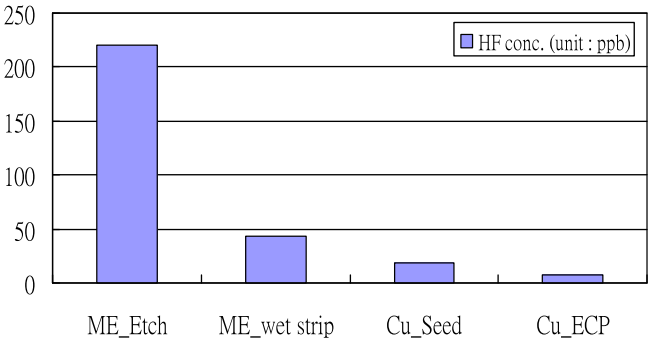

Fig. 9. Distribution of HF concentration out-gases after various BEOL processing in ULSI manufacturing.

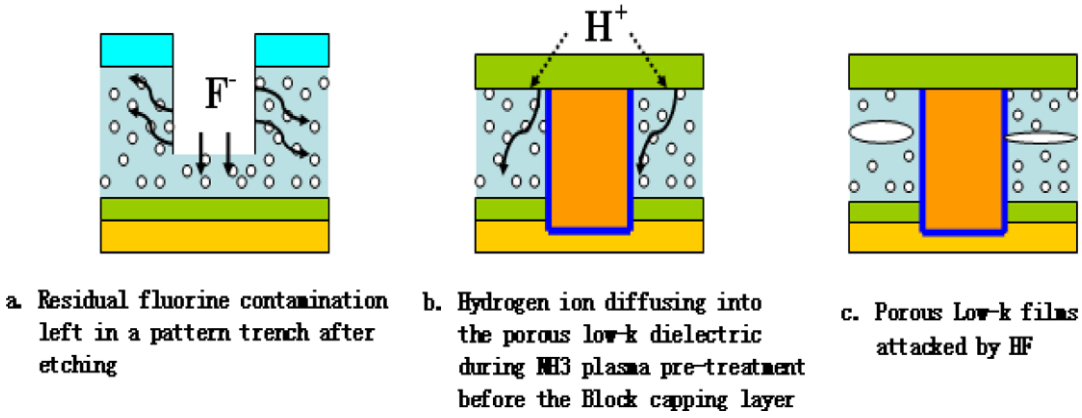

Fig. 10. The illustrations for voltage ramping-up to dielectric breakdown failure model during integrated fabrication.

(2*T*) shows better line-to-line leakage current than that of the standard one (1*T*). There are several important implications of this result. Fist of all, this data suggests that the enhanced UV curing produces a well-fabricated Si–O–Si structure with high mechanical strength and appropriately low dielectric constant. Secondly, the line-to-line spacing of meander-fork pattern would be changed, because the line width is changed with different UV curing process on low-*k* dielectrics. Fig. 6a and b show that the graphs of the TEM in the Static Random Access Memory (SRAM) region for standard UV curing sample and enhanced curing one. A percolation path created in the space of SRAM region for standard UV curing sample can be seen in the cross-sectional TEM micrograph shown in Fig. 6a. Fig. 7 shows the distributions of the line resistance in a single damascene architecture, Cu with the porous low-*k* interconnections. The Cu line resistance was increased slightly because of its smaller line width for an enhanced UV curing condition. The average intra-level voltage ramping-up to dielectric breakdown of the standard UV curing sample with a value of 12.2 voltage was 18.853% lower than that of the enhanced UV curing one with a value of 14.5 voltage. We demonstrated that the inter-level VRDB failure mechanism relies on UV curing conditions on this porous low-*k* dielectric.

Studies [3,16] have reported that the quality of the interface between a dielectric oxide barrier and the underlying films are related to the electrical breakdown strength. The interfacial characteristics between a dielectric oxide barrier and the underlying film were influenced by not only the adhesion strength between both materials but also the pre-treatment on the underlying film. Noguchi [16] reported that NH_3 plasma heals the damage on the surface of Cu and porous dielectrics by forming a nitride layer on the Cu surface and Si–H and Si–N bonds on the dielectric surface, thus improving the electrical performance. Fig. 8 shows the distributions of voltage ramping-up to dielectric breakdown for various NH_3 plasma pre-treatment conditions before SiCN capping. Non-NH_3 plasma pre-treatment has better voltage ramping-up to dielectric breakdown performance. This result seems to contradict previous studies, but thermal annealing may have prevented damage after CMP in our study. Moreover, double NH_3 plasma pre-treatment obviously degrades the performance of voltage ramping-up to dielectric breakdown. It is inferred that some factors of NH_3 plasma pre-treatment on underlying films deteriorate the electrical performance.

Fig. 9 shows the distribution of HF concentration out-gases after various BEOL processes in ULSI manufacturing. The etching process used fluorine-based chemistries to pattern the trench profile. In addition, the fluorine-based chemistries dissociated, and then the residue of fluorine ion on the surface of the sidewall is considered. Hence, high HF concentration out-gases was also found after this etching process. Fig. 10 shows the illustration of voltage ramping-up to dielectric breakdown failure model during integrated fabrication. Porous low-*k* dielectric degradation during fabricated integration is caused by a combination of two factors: first is the residual fluorine contamination left in a pattern trench after etching; second is hydrogen ion diffusing into the porous low-*k* dielectric during NH_3 plasma pre-treatment before the SiCN capping layer. The residual fluorine and hydrogen ions react and then damage the inner porous structures, increasing the film porosity. This is explained why a percolation path was found in the porous low-*k* dielectric layer due to the damage from HF corrosion. The greater porosity forms more defective sites which create a percolation path under an applied electrical stress [17], then Cu easily penetrated it. As a result, dielectric breakdown easily fails under an enhanced electric field.

4. Conclusions

The introduction of porosity into low-*k* dielectric interconnections introduces more challenges for the reliability in or beyond 45 nm node devices. In conclusion, the dominant failure mechanism for both the lower voltage-ramped breakdown and higher leakage current was that more electrons easily transported through the percolation path in intra-layer porous low-*k* materials damaged from HF corrosion. Moreover, an optimal ultraviolet curing process (Enhanced UV curing) and less NH_3 plasma pre-treatment on porous low-*k* dielectrics before a SiCN capping layer is developed improving the electrical performance in both cases. This is believed to be the result of the stiff configurations of the reconstruction of Si–O network structures and lower HF damage made. These reconstruction structures preserve its pore architectures and suppress the damage from the HF. In our study, the proposed failure model from integrated processes facilitates the understanding of the reliability issue and provides valuable fabrication data for well-built interconnections of back-end of line (BEOL) in or beyond 45 nm node devices.

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References

[1] R. Gonella, P. Motte, J. Torres, Microelectron. Reliab. 40 (2000) 1305–1309.
[2] E.T. Ogawa, J. Kim, G.S. Haase, H.C. Mogul, J.W. McPherson, in: Proc. Int. Reliability Physics Symp., 2003, pp. 166–171.

[3] Gleen B. Alers, K. Jow, R. Shaviv, G. Errit Kooi, G.W. Ray, IEEE Trans. Dev. Mater. Reliabil. 4 (2004) 148–152.
[4] J. Noguchi, N. Konishi, Y. Yamada, IEEE Trans. Electr. Dev. 52 (2005) 934–941.
[5] C.L. Cornec, F. Ciaramella, V. Jousseaume, P. Leduc, A. Zenasni, G. Passemard, Microelectron. Eng. 83 (2006) 2122–2125.
[6] P. Verdonck, D.D. Roest, S. Kaneko, R. Caluwaerts, N. Tsuji, K. Matsushita, N. Kemeling, Y. Travaly, H. Sprey, M. Schaekers, G. Beyer, Surf. Coat. Technol. 201 (2007) 9264–9268.
[7] V. Jousseaume, L. Favennec, A. Zenasni, G. Passemard, Appl. Phys. Lett. 88 (2006) 182908–182912.
[8] L. Favennec, V. Jousseaume, G. Gerbaud, A. Zenasni, G. Passemard, J. Appl. Phys. 102 (2007) 064107–064116.
[9] S. Lee, J. Yang, S. Yeo, J. Lee, D. Jung, J.H. Boo, H. Kim, H. Chae, Jpn. J. Appl. Phys. 46 (2007) 536–541.
[10] Chery D. Hartfield, Ennis T. Ogawa, Y.J. Park, T.C. Chiu, H. Guo, IEEE Trans. Dev. Mater. Reliabil. 4 (2004) 129–140.
[11] S.I. Nakao, J. Ushio, T. Ohno, T. Hamada, Y. Kamigaki, M. Kato, K. Yoneda, S. Kondo, N. Kobuyashi, in: IEEE Int. Interconnect Technology Conf., 2006, p. 66.
[12] J. Ushio, T. Ohno, T. Hamada, S.I. Nakao, K. Yoneda, M. Kato, N. Kobayashi, J. Appl. Phys. 46 (2007) L405.
[13] C.H. Huang, H.L. Huang, C.I. Hung, N.F. Wang, Y.H. Wang, M.P. Houng, Jpn. J. Appl. Phys. 47 (2008) 1532.
[14] Y. Shioya, H. Shimoda, K. Maeda, T. Ohdaira, R. Suzuki, Y. Seino, Jpn. J. Appl. Phys. 44 (2005) 3879–3884.
[15] F. Ciaramella, V. Joussenaume, S. Maitrejean, M. Verdier, B. Remiat, G. Passemard, Thin Solid Films 495 (2006) 124–129.
[16] J. Noguchi, N. Ohashi, J. Yasuda, T. Jimbo, H. Yamaguchi, N. Owada, K. Takeda, K. Hinode, in: Proc. IRPS, 2000, pp. 339–343.
[17] C. Hong, L. Milor, Microelectron. Reliab. 47 (2007) 1478–1482.